intel

*Development Solutions*

# ICE™-5100/252
# User Probe Supplement

Order Number: 167097-002

## Notational Conventions

| | |
|---|---|
| italics | are for variable expressions. You substitute a value or symbol. |
| {*items*} | between braces indicate that you must select one and only one item in the enclosed menu. |
| [*items*] | between brackets are optional items of which you can select one and only one. |
| <CNTL> | denotes the host keyboard's control key. For example, <CNTL>C means enter C while pressing the control key. |
| *device* | stands for the letter or number of a disk drive. |
| *dirname* | stands for any directory created by a user. |
| *filename* | is a valid file name. |
| *pathname* | specifies a path to a file. It can include *device*, *dirname*, and *filename*. |
| punctuation | other than ellipses (. . .), braces ({ }), and brackets ([ ]) must be entered exactly as shown. |
| `shading` | is used in examples to show user input. |
| UNDERSCORE | is used to show valid abbreviations used for commands. |

# ICE™-5100/252 USER PROBE SUPPLEMENT

Order Number: 167097-002

| REV. | REVISION HISTORY | DATE |
|---|---|---|
| -001 | Original Issue. | 8/86 |
| -002 | Final Typeset Version. | 9/86 |


Intel Corporation, 3065 Bowers Avenue, Santa Clara, California 95051

**CAUTION**

This equipment generates, uses, and can radiate radio frequency energy and if not installed and used in accordance with the instruction manual, may cause interference to radio communications. As temporarily permitted by regulation, it has not been tested for compliance with the limits for Class A Computing Devices pursuant to Subpart J of Part 15 of FCC rules, which are designed to provide reasonable protection against such interference. Operation of this equipment in a residential area is likely to cause interference in which case the user, at his own expense, will be required to take whatever measures may be required to correct the interference.

Additional copies of this manual or other Intel literature may be obtained from:

Intel Corporation
Literature Sales
P.O. Box 58130
Santa Clara, CA 95052-8130

Intel Corporation makes no warranty of any kind with regard to this material, including, but not limited to, the implied warranties of merchantability and fitness for a particular purpose. Intel Corporation assumes no responsibility for any errors that may appear in this document. Intel Corporation makes no commitment to update nor to keep current the information contained in this document.

Intel Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in an Intel product. No other circuit patent licenses are implied.

Intel software products are copyrighted by and shall remain the property of Intel Corporation. Use, duplication or disclosure is subject to restrictions stated in Intel's Software License Agreement, or in the case of software delivered to the government, in accordance with the software license agreementas defined in FAR 52.227-7013.

No part of this document may be copied or reproduced in any form or by any means without prior written consent of Intel Corporation.

Intel Corporation retains the right to make changes to these specifications at any time, without notice.

Contact your local sales office to obtain the latest specifications before placing your order.

The following are trademarks of Intel Corporation and its affiliates and may be used only to identify Intel products:

| | | | |
|---|---|---|---|
| Above | $i_m$ | iSBC | PC BUBBLE |
| BITBUS | iMDDX | iSBX | Plug-A-Bubble |
| COMMputer | iMMX | iSDM | PROMPT |
| CREDIT | Insite | iSXM | Promware |
| Data Pipeline | Intel | KEPROM | QueX |
| FASTPATH | $int_el$ | Library Manager | QUEST |
| GENIUS | $int_elBOS$ | MAP-NET | Quick-Pulse Programming |
| $\Delta$ | Intelevision | MCS | Ripplemode |
| i | $int_eligent$ Identifier | Megachassis | RMX/80 |
| i | $int_eligent$ Programming | MICROMAINFRAME | RUPI |
| $I^2ICE$ | Intellec | MULTIBUS | Seamless |
| ICE | Intellink | MULTICHANNEL | SLD |
| iCEL | iOSP | MULTIMODULE | UPI |
| iCS | iPDS | ONCE | VLSiCEL |
| iDBP | iPSC | OpenNET | 4-SITE |
| iDIS | iRMX | OTP | |
| iLBX | | | |

MDS is an ordering code only and is not used as a product name or trademark. MDS® is a registered trademark of Mohawk Data Sciences Corporation.

IBM is a registered trademark of International Business Machines Corporation.

MULTIBUS® is a patented Intel bus.

# CONTENTS

# PREFACE

This manual is divided into the following chapters:

| | |
|---|---|
| Chapter 1 | describes ICE™-5100/252 user probe design considerations. |
| Chapter 2 | describes the ICE-5100/252 user probe commands and keywords. |
| Appendix A | describes the customer confidence tests for the ICE-5100/252 user probe. |
| Appendix B | lists the ICE-5100/252 special function registers. |
| Appendix C | lists the ICE-5100/252 special function register bits. |
| Appendix D | describes the differences in CHMOS and HMOS components and how the ICE-5100/252 user probe supports these parts. |

# 1 DESIGN CONSIDERATIONS

## 1.1 Introduction

This chapter describes design considerations you should be aware of when using the ICE™-5100/252 user probe. Refer to the *ICE-5100 Emulator Installation Supplement*, order number 167095, for instructions on connecting your user probe components together and to a host computer system.

**CAUTION**

The ICE-5100/252 user probe contains CHMOS components. Be sure you follow proper electrostatic discharge procedures during installation and handling.

As shown in Figure 1-1, the ICE-5100/252 user probe consists of the following components:

- Processor Module — The processor module houses the emulation processor, buffer ICs, user cable connector, two 36-pin iSBX™ connectors, and a 10-pin connector which is used to connect test equipment to the emulator.
- User Cable — The user cable is approximately 1 meter (3 feet) in length. One end of the user cable connects to the procesor module and the other end of the cable connects to the ICE-5100 controller pod.
- Crystal Power Accessory — The crystal power accessory (CPA) is a small detachable printed circuit board that enables you to use the emulator in a stand-alone mode of operation. The CPA provides clock and power to the user probe.

  The CPA is also used when executing the ICE-5100/252 customer confidence tests.

**NOTE**

A target adaptor is needed before you can connect your ICE-5100/252 user probe to a target system. The target adaptor mounts to the bottom of the processor module and provides pin for pin compatibility with target system sockets. Target adaptors based on different package types are available.

## 1.2 MCS®-51 Microcontroller Support Offered by ICE™-5100/252 User Probe

The ICE-5100/252 user probe can emulate the microcontrollers listed in Table 1-1.

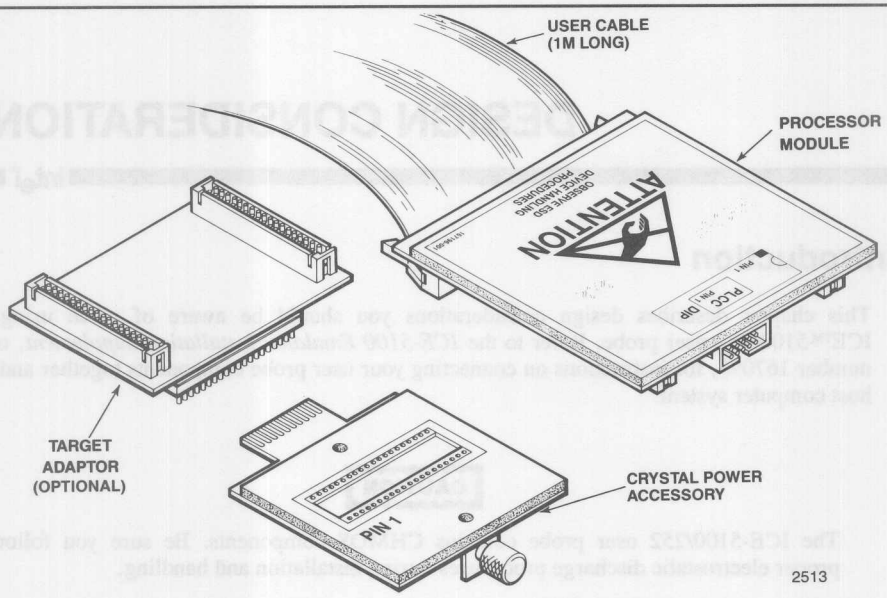



**Figure 1-1 ICE™-5100/252 User Probe Components**

**Table 1-1 MCS®-51 Family Support Offered by the ICE™-5100/252 Emulator**

| Part | On-Chip Program Memory | On-Chip Data Memory |
|---|---|---|
| 8031 | None | 128 bytes |
| 80C31 | None | 128 bytes |
| 8032 | None | 256 bytes |
| 8051 | 4KB-ROM | 128 bytes |
| 80C51 | 4KB-ROM | 128 bytes |
| 8052 | 8KB-ROM | 256 bytes |
| 80C252 | None | 256 bytes |
| 83C252 | 8KB-ROM | 256 bytes |
| 8751 | 4KB-EPROM | 128 bytes |
| 87C51 | 4KB-EPROM | 128 bytes |
| 8752 | 8KB-EPROM | 256 bytes |
| 87C252 | 8KB-EPROM | 256 bytes |

## 1.3 Processor Module Dimensions

The height of the processor module and target adaptor may pose a problem for multiple board target systems that need to be debugged. Allow at least 1-1/2 inches (3.8 cm) of space between boards to fit the processor module and a target adaptor.

Refer to Figure 1-2 for the dimensions of the processor module.

## 1.4 Emulation of CHMOS and HMOS Components

The ICE-5100/252 user probe is based on a CHMOS emulation processor and can emulate the CHMOS and HMOS components listed in Table 1-1. The user probe comes configured for emulating CHMOS components and HMOS components using an internal clock (crystal).

Refer to Appendix D for information on how the ICE-5100/252 user probe supports emulation of CHMOS and HMOS components.

## 1.5 Changing the Jumpers on the Processor Module

If you plan to emulate HMOS components using an external clock, you must move the jumpers located on the bottom of the processor module and execute the CPU command (described in Chapter 2).

Perform the following steps to change the jumpers on the processor module.

1. Remove the target adaptor from the processor module by inserting a small-blade screwdriver into one of the four slots between the processor module and the target adaptor and turning gently (refer to Figure 1-3). Repeat this process on the remaining three slots and remove the target adaptor.

2. Referring to Figure 1-4, set the jumpers (E1-E8) according to the type of component you are emulating.

3. Connect the target adaptor to the processor module by aligning the connectors on the target adaptor with the iSBX connectors on the processor module (refer to Figure 1-5). The two iSBX connectors are keyed to prevent improper installation of the target adaptor.

   Press the two connectors firmly together until all four corners of the target adaptor are locked to the processor module.

4. Execute the CPU command to configure the ICE-5100/252 emulator software around the type of component selected.

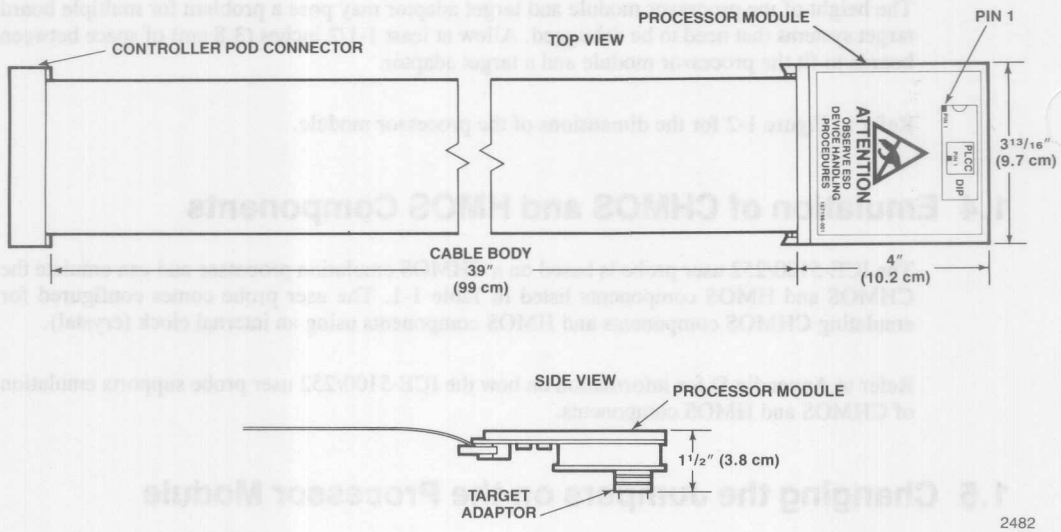



**Figure 1-2 Processor Module Dimensions**

## 1.5.1 Example of Changing Jumpers on the Processor Module

To emulate one of the HMOS components listed in Table 1-1 using an external clock, set the jumpers on the processor module as follows:

| Jumpers Installed | Jumpers Removed |
|---|---|
| E1 - E2 | E5 - E6 |
| E3 - E4 | E7 - E8 |

Enter the following CPU command to configure the software:

```
hlt> CPU = H52      (Selects the 8052 HMOS family)
```

or

```
hlt> CPU = H51      (Selects the 8051 HMOS family)
```

To emulate a CHMOS component or an HMOS component using internal clock (crystal), set the jumpers on the processor module as follows:

| Jumpers Installed | Jumpers Removed |
|---|---|
| E5 - E6 | E1 - E2 |
| E7 - E8 | E3 - E4 |

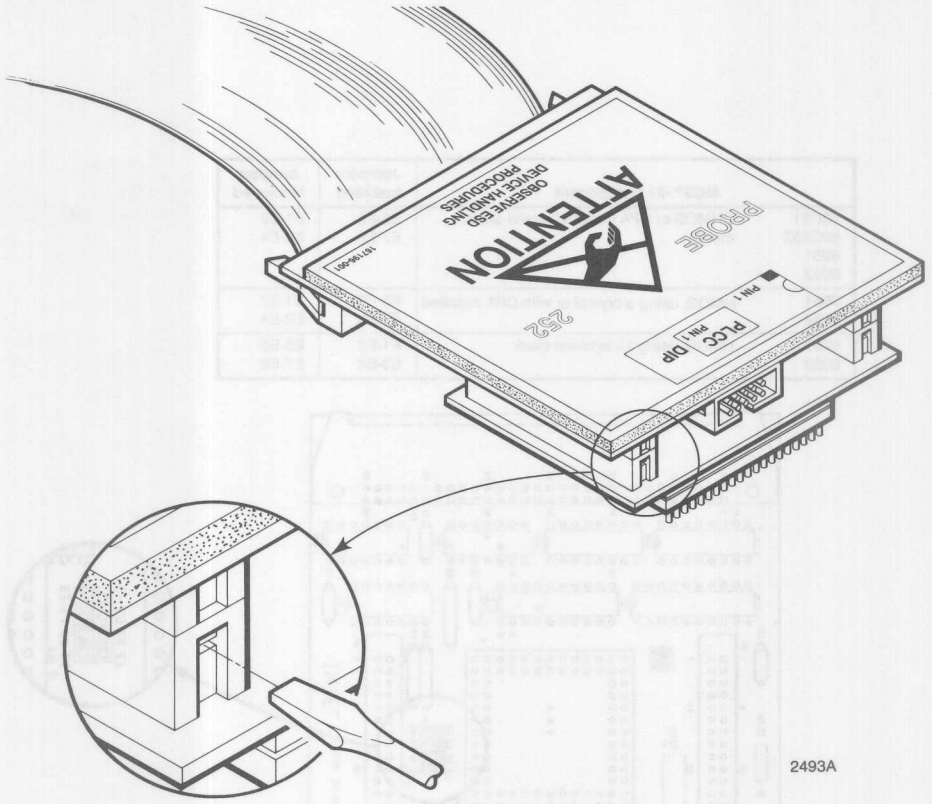



**Figure 1-3 Removing the Target Adaptor**

Enter the following CPU command to configure the software:

```
hlt> CPU = C252
```
(Selects the 80C252 CHMOS family)

or

```
hlt> CPU = C51
```
(Selects the 80C51 CHMOS family)

or

```
hlt> CPU = H51
```
(Selects the 8051 NMOS family)

| MCS® -51 Component | | Jumpers Installed | Jumpers Removed |
|---|---|---|---|
| 80C51<br>80C252<br>8051<br>8052 | CHMOS or CPA installed (stand-alone mode) | E5-E6<br>E7-E8 | E1-E2<br>E3-E4 |
| 8051<br>8052 | HMOS, using a crystal or with CPA installed | E5-E6<br>E7-E8 | E1-E2<br>E3-E4 |
| 8051<br>8052 | HMOS, using an external clock | E1-E2<br>E3-E4 | E5-E6<br>E7-E8 |

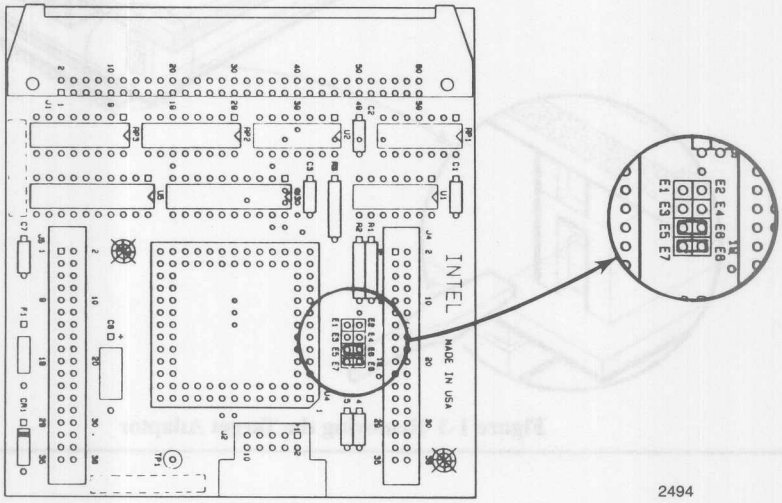



**Figure 1-4 Processor Module Jumpers**

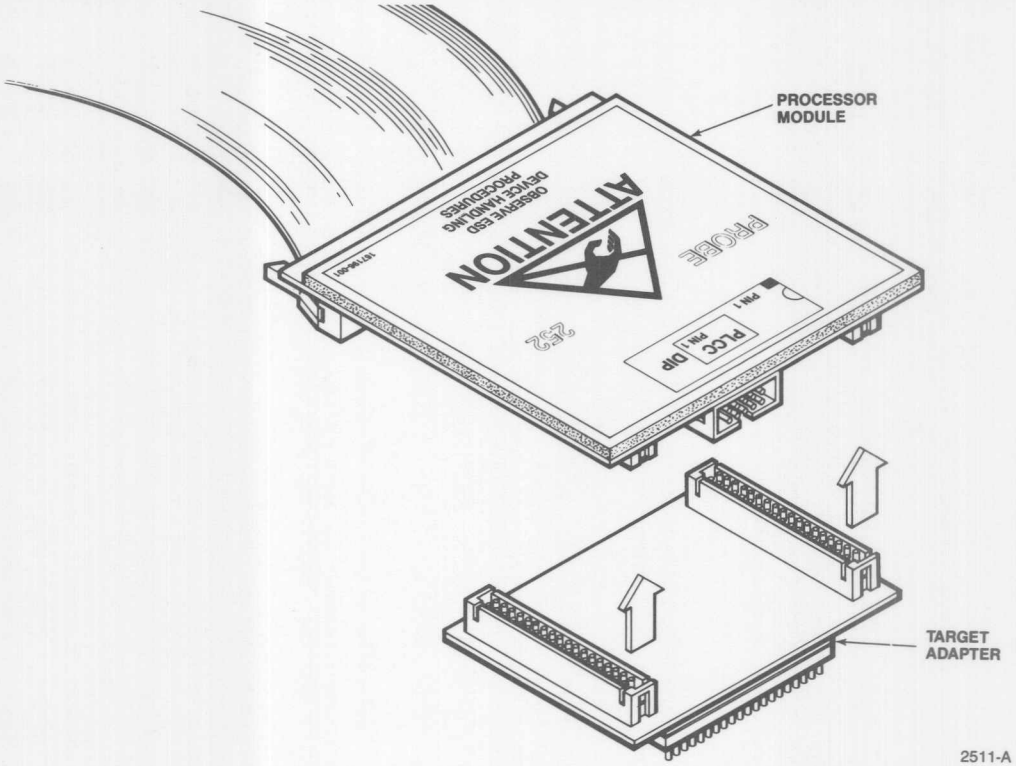



**Figure 1-5 Connecting the Target Adaptor to the Processor Module**

# 2 ICE™-5100/252 USER PROBE COMMANDS

## Introduction

This chapter describes the user probe commands. It contains a list of ICE-5100/252 user probe keywords. Table 2-1 lists the commands by function along with the page on which they appear.

## Syntax Notation

The following notation is used throughout the chapter.

*italics* are for variable expressions. You substitute a value or symbol.

{*items*} between braces indicate that you must select one and only one item in the enclosed menu.

[*items*] between brackets are optional items of which you can select one and only one.

punctuation other than braces ({ }) and brackets ([ ]) must be entered exactly as shown.

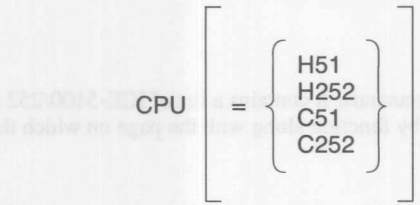
**Table 2-1 ICE™-5100/252 User Probe Commands**

| Function | Command | Page | Description |
|---|---|---|---|
| Processor Type | CPU | 2-2 | Displays or modifies the processor type being emulated. |
| ICE-5100/252 Keywords | Keywords | 2-4 | Lists the words and symbols reserved for use by the ICE-5100/252 user probe. |
| Registers | *sfr*<br>*sfr-bit* | 2-5<br>2-7 | Displays or modifies one of the special function registers.<br>Displays or modifies one of the special function register bits. |

# CPU

Displays or changes the processor type being emulated

## Syntax




Where:

CPU displays the current processor type being emulated. The default processor type is the 80C252 microcontroller.

H51 selects the 8051 HMOS family of microcontrollers.

H52 selects the 8052 HMOS family of microcontrollers.

C51 selects the 80C51 CHMOS family of microcontrollers.

C252 selects the 80C252 CHMOS family of microcontrollers. This is the default processor type for the ICE-5100/252 user probe.

## Discussion

Use the CPU command to display or change the processor type being emulated.

Changing the processor type affects the processor characteristics shown in Table 2-2.

The processor type is not affected by a RESET command and can only be changed via the CPU command. Changing the processor type resets the memory map to the default map for the selected processor. CPU also defines the special function register keywords that are valid for each family of processors (see Appendix B).

**WARNING**

All special function registers are available during emulation regardless of the CPU selected. Accidental manipulation of PCA control bits while in 8051 mode can cause unexpected interrupts.

Entering CPU without specifying a *cpu-value*, displays the current processor type being emulated.

**Table 2-2 Processor Characteristics Affected by the CPU Command**

| CPU | Bytes of RAM | Bytes of ROM | EA/ ROM Security | Framing Error Detection | Power-Down Reduction Mode | Power-Down Exit by External Interrupt |
|---|---|---|---|---|---|---|
| H51 | 128 | 4K | NO | NO | NO | NO |
| H52 | 256 | 8K | NO | NO | NO | NO |
| C51 | 128 | 4K | NO | NO | YES | NO |
| C252 | 256 | 8K | YES | YES | YES | YES |

### Emulation of HMOS Components

If you are emulating an HMOS component using an external clock, you will have to move the jumpers on the bottom of the processor module. Refer to Section 1.5 in this manual for the correct jumper configuration.

## Examples

1. Display the current CPU processor type.

```
hlt> CPU
C252
```

2. Change the processor type to the 8051 HMOS microcontroller.

```
hlt> CPU = H51
WARNING: Map has been reset.
```

# Keywords

## Words reserved for use by the ICE-5100/252 user probe

The ICE-5100/252 user probe uses the following words and symbols. These are in addition to the keywords listed in Chapter 3 of the *ICE™-5100 Emulator Reference Manual*, order number 166257.

Do not define a debug symbol to have the same name as a keyword. If your program has a variable or procedure name that duplicates a keyword, use the quote (") operator when you reference that variable or procedure name (for example, "CPU). Refer to Appendix B and C for a listing of Special Function Register (SFR) keywords.

C252 C51 CPU H51 H52

# Special Function Registers

Displays or modifies an addressable special function register

## Syntax

$$\left\{ \begin{array}{l} sfr\ [=\ expression] \\ .sfr \end{array} \right\}$$

Where:

| | |
|---|---|
| *sfr* | is a valid special function register keyword for the selected processor type. (Appendix B lists the special function registers). |
| *expression* | resolves to a byte value. |
| *.sfr* | returns the address of the specified special function register. |

## Discussion

Use the special function register keywords to display or modify special function register values or to display the address of a register.

Entering a register keyword by itself displays the current value of the register. All individual registers are displayed in the current base. The CPU command determines which register keywords are valid for each processor type.

## Examples

1. Display the contents of the ACC register.

```
hlt> ACC
0AH
```

2. Modify the contents of the ACC register.

```
hlt> ACC=0FFH
```

3. Display the address of the CCON register.

```
hlt> .CCON
RDATA 00D8H
```

## Cross-Reference

CPU
Special Function Register Bits

# Special Function Register Bits

Displays or modifies an addressable special function register bit

## Syntax

{ *sfr-bit* [ = expression]
*sfr.bit-num* [ = expression]
*.sfr-bit*
*.sfr.bit-num* }

Where:

| | |
|---|---|
| *sfr-bit* | is a valid special function register bit keyword for the selected processor type. (Appendix C lists the register bit keywords.) |
| *sfr* | is a valid special function register keyword for the selected processor type. (Appendix B lists the special function registers.) |
| *expression* | resolves to a bit value of 0 or 1. |
| *bit-num* | is any valid number (0-7). |
| *.sfr-bit or .sfr.bit-num* | returns the address of the special function register bit. |

## Discussion

Use the special function register bit keywords to display or modify special function register bit values or to display the address of a bit.

Entering a register bit keyword by itself displays the current value of the register bit. The CPU command determines which register bit keywords are valid for each processor type.

## Examples

1. Modify the CY bit of the PSW register.

```
hlt> CY=01H
```

2. Display the address of the CF bit.

```
hlt> .CF
BIT 00DFH
```

3. Modify bit 2 of register P0.

```
hlt> P0.2 = 0
```

## Cross-Reference

CPU
Special Function Registers

# A CUSTOMER CONFIDENCE TESTS

## A.1 INTRODUCTION

The customer confidence tests check the operation of the ICE™-5100/252 user probe and the ICE-5100 controller pod. Run the confidence tests after installation and whenever you suspect the emulator is not operating properly.

In order to run the customer confidence tests, the ICE-5100/252 CPA must be connected to the controller pod and the ICE-5100/252 user probe plugged into the CPA as shown in Figure A-1.

**CAUTION**

The ICE-5100/252 user probe contains CMOS components. Be sure you follow proper electrostatic discharge procedures while installing or handling the user probe.

Separate sections are provided on the following topics:



## A.2 Invoking The Confidence Tests

To load the confidence tests, perform the following steps.

1. Turn on the ICE-5100/252 emulator, host computer system, and any peripheral devices required.
2. Boot the host operating system.
3. Insert the disk labeled ICT252 ICE-5100/252 Confidence Tests into an available floppy disk drive. Be sure you have the correct disk for your user probe.

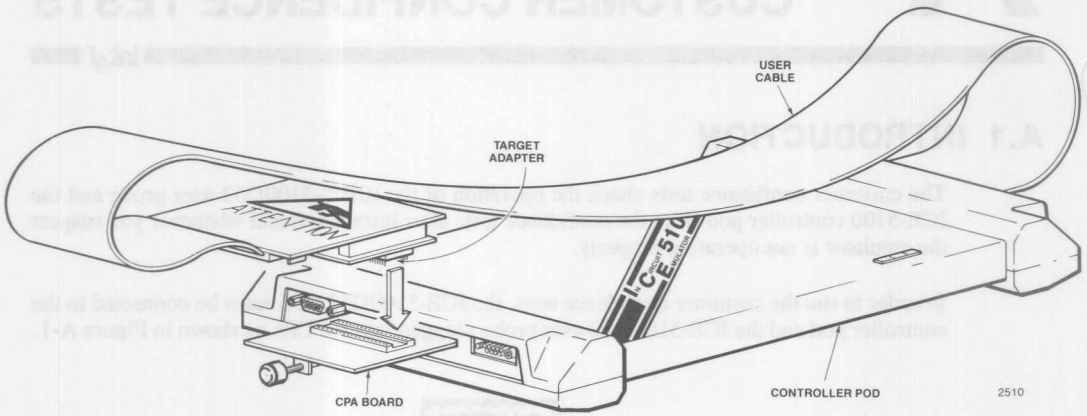



**Figure A-1 Proper Configuration for Running the Confidence Tests**

4. Enter the following command to invoke the confidence test software (Series III hosts require RUN to be entered before the command):

   [RUN] *pathname* ICT252

   After the confidence test software loads, the following display appears on the screen:

```
host-name ICT-252 Customer Confidence Test Vx.y
Copyright 1986 Intel Corporation
}
```

## A.3 Selecting a Non-Default Baud Rate

The default baud rate for running the confidence tests is 9600. Table A-1 shows optional settings for the baud rate.

The diagnostic variable V(E) sets the optional baud rate. V(E) does not take effect until the software is reset. To change the baud rate, enter the following commands (in the command, *n* refers to one of the baud rate selection numbers in Table 3-1):

```
}V(E) = n
}RESET
```

**Table A-1 Optional Baud Rates**

| V(E) | Baud Rate |
|---|---|
| 0, 1 | 300 |
| 2, 3, 4 | 1200 |
| 5 | 9600 |
| 6 | 19200 |

**NOTE**

All confidence test commands can be abbreviated to the first three characters of the command. For example, RESET can be abbreviated to RES.

To display the contents of any global variable, enter the variable name. For example:

```
}DEBUG      (displays the current setting of this variable)
}V(E)       (displays the baud rate)
```

## A.4 Running the Confidence Tests

To run the confidence tests, perform the following steps:

1. To start the confidence tests, enter:

   ```
   }TEST
   ```

   The confidence tests take approximately four minutes to complete. If all tests pass, the prompt (}) reappears on the screen. At this point, you are ready to exit the confidence test software.

**CAUTION**

Do not remove the confidence test disk while testing is in progress.

2. If a confidence test causes the system to hang, correct the problem by entering:

   Intel hosts:

   ```
   }<CNTL>C
   }RESET
   ```

   IBM hosts:

   ```
   }<CNTL><BREAK>
   }RESET
   ```

3. If any of the confidence tests fail, you can obtain a summary of failing tests by entering

```
}SUMMARY EO
```

Contact your Intel product service center if the ICE-5100/252 emulator does not pass the confidence tests. (Refer to the inside back cover for service information.)

4. To exit from the confidence test software, enter

```
}EXIT
```

## A.5 Confidence Test Error Messages

The confidence tests display the following three message types:

- Test name — describes the function being tested.
- Status message — describes events or intermediate results within the test currently running.
- Error message — describes a detected fault.

By default, the confidence tests provide the test name and a PASS/FAIL message. You can request more information by setting the software flags DEBUG and ERRONLY. Table A-2 shows how the confidence tests interpret the DEBUG and ERRONLY flags.

To display the current values for these flags, enter:

```
}QUERY
```

The system will display the settings of the DEBUG and ERRONLY flags.

Change the DEBUG and ERRONLY flags by resetting their values. For example, to set the DEBUG flag to TRUE, enter

```
}DEBUG = 1
```

**Table A-2 The DEBUG and ERRONLY Flags**

| DEBUG | ERRONLY | Description |
|---|---|---|
| 0 | 0 | Prints all test names; prints PASS/FAIL messages. The default is 00. |
| 1 | 0 | Prints all test names; prints all status and error messages. |
| 0 | 1 | Prints only the name of those tests that failed; prints no status or error messages. |
| 1 | 1 | Prints only the names of those tests that failed; prints error messages. |

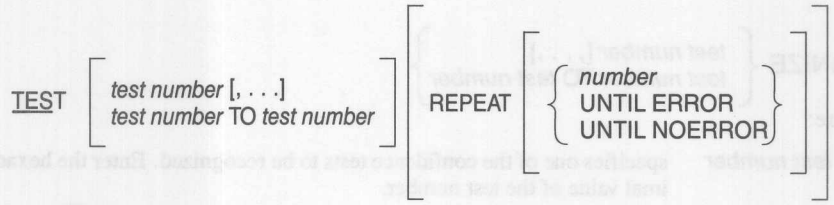
## A.6 Confidence Test Commands

The following sections describe the confidence test commands and their syntax. You can use these commands to control the execution of the confidence tests. (The underlined portion of the command indicates the valid abbreviation for the command.)

You can enter numeric values for these commands in hexadecimal (H), decimal (T), octal (Q), or binary (Y) by attaching the appropriate suffix to the value. The default base (if no suffix is given) is hexadecimal.

### A.6.1 TEST

**Syntax**




Where:

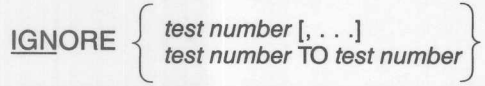
| | |
|---|---|
| *test number* | specifies one of the confidence tests to be executed. Enter the hexadecimal value of the test number. |
| REPEAT | specifies that the test is to loop. If REPEAT is not followed by FOREVER, a *number*, or UNTIL, the default REPEAT FOREVER is assumed. |
| FOREVER | specifies that the test is to be executed forever |
| *number* | specifies the number of times the test is to be executed. |
| UNTIL ERROR | specifies that the test is to be executed until an error occurs. |
| UNTIL NOERROR | specifies that the test is to be executed until no errors occur. |

**Discussion**

The TEST command causes the specified test(s) to be executed one or more times.

### A.6.2 IGNORE

**Syntax**



Where:

*test number* specifies one of the confidence tests to be ignored. Enter the hexadecimal value of the test number.

### Discussion

The IGNORE command enables you to specify a test or tests to be ignored. Ignored tests are not executed.

## A.6.3 RECOGNIZE

### Syntax

RECOGNIZE { *test number* [, . . .] | *test number* TO *test number* }

Where:

*test number* specifies one of the confidence tests to be recognized. Enter the hexadecimal value of the test number.

### Discussion

The RECOGNIZE command allows the user to declare the specified test or tests to be recognized and run.

## A.6.4 DESCRIBE

### Syntax

DESCRIBE { *test number* [, . . .] | *test number* TO *test number* }

Where:

*test number* specifies one of the confidence tests to be described. Enter the hexadecimal value of the test number.

### Discussion

The DESCRIBE command prints the name and number of the specified test or tests.

## A.6.5 CLEAR

### Syntax

CLEAR { *test number* [, . . .] | *test number* TO *test number* }

Where:

*test number* specifies one of the confidence tests to be cleared. Enter the hexadecimal value of the test number.

### Discussion

The CLEAR command clears the execution count and error count to zero for the specified tests. The execution count is the number of times the specified tests have been run and the error count is the number of errors detected. If no tests are specified, the CLEAR command clears the count for all the tests.

## A.6.6 RESET

### Syntax

RESET { software | hardware }

Where:

software specifies that the software is to be reset.

hardware specifies that the hardware is to be reset.

### Discussion

The RESET command allows the user to reset software and hardware to their initial state. RESET used without specifying SOFTWARE or HARDWARE will first reset the software and then reset the hardware.

## A.6.7 SUMMARY

### Syntax

SUMMARY { *test number* [, . . .] [EO] | *test number* TO *test number* }

Where:

*test number* specifies the confidence tests to be summarized. Enter the hexadecimal value of the test number.

### Discussion

The SUMMARY command displays the results log for the specified tests. The log includes the number and names of the test followed by the number of times it was executed and the number of passes and failures.

## A.6.8 LIST

### Syntax

LIST {*filename*}

Where:

*filename* specifies the name of a file to be used.

### Discussion

The LIST command causes all console activity to be logged in the specified file. The file will contain a log of all interaction between the test monitor and the user. If no *filename* is specified, the current open list file is closed.

### Example

```
LIST :fl:results.log
LIST :lp:
```

## A.6.9 QUERY

### Syntax

QUERY

### Discussion

The QUERY command displays the current state of the test managers DEBUG and ERRONLY.

## A.6.10 EXIT

### Syntax

EXIT

### Discussion

The EXIT command ends the test session and returns control back to the operating system.

## A.7 List of Confidence Tests

Table A-3 lists the individual confidence tests.

**Table A-3 List of Confidence Tests**

| Test Number | Test Name | Description |
|---|---|---|
| 0000H | Communication Synchronization | Verifies system synchronization and data transfer. |
| 0001H | Host Serial Loopback (Usually Ignored) | Verifies the host serial hardware and cable operation. The Txd pin must loop back into the Rxd pin. |
| 0002H | Probe ID Verification | Verifies the READ command and the version number of the controller firmware. |
| 0003H | Controller RAM | Verifies the accessibility, address uniqueness, and data integrity of the control processor RAM. |
| 0004H | Pod Temperature Sensor Check | Verifies that the emulator is operating within the specified temperature range. |
| 0005H | Trace Memory RAM | Verifies the accessibility, address uniqueness, and data integrity of the trace memory RAM. |
| 0006H | Break Memory RAM | Verifies the accessibility, address uniqueness, and data integrity of the break memory RAM. |
| 0007H | Command Memory RAM | Verifies the accessibility, address uniqueness, and data integrity of the command memory RAM. |
| 0008H | Trace Qualification Memory | Verifies the accessibility, address uniqueness, and data integrity of the trace qualification memory RAM. |
| 0009H | Emulation Memory | Verifies the accessibility, address uniqueness, and data integrity of the emulation memory RAM. This test takes approximately 45 seconds to execute. |
| 000AH | MAP Memory RAM | Verifies the accessibility, address uniqueness, and data integrity of the MAP memory RAM. |
| 000BH | BUSY/DONE/STOP/ABORT | Verifies that the BUSY/DONE bits properly report the ICE status, that the STOP bit can halt the emulation and command sequence, and that the ABORT bit can halt an emulation sequence. |
| 000CH | Break/Command Multiplexor | Verifies the selection of break/command RAM pages by the address multiplexor and address line 8 (A8). |
| 000DH | Trace Counter | Verifies the accessibility and proper operation of the trace address counter and that the overflow flag bit can be set and cleared. |
| 000EH | Break Armed | Verifies that the appropriate control bits in the control register operate correctly and that an emulation sequence affects the level of this status bit. |
| 000FH | Break Synchronization | Verifies that a match between an execution address and a break setting causes emulation to halt immediately. |
| 0010H | Break Detection Inputs | Verifies the operation of the four input pairs to the break detection circuit. |

**Table A-3 List of Confidence Tests continued**

| Test Number | Test Name | Description |
|---|---|---|
| 0011H | Trace Active Status | Verifies that the appropriate control bits in the control register operate correctly and that an emulation sequence with the appropriate trace qualification memory bits set will affect the status of this bit. |
| 0012H | Trace Enable Inputs | Verifies the operation of the three input pairs to the trace qualification circuits and the operation of the range trace qualification (RTE) control bit. |
| 0013H | Interrogation Control | Verifies that interrogation word 1 (INTR1) reflects the correct processor status. |
| 0014H | Memory Size | Verifies the operation of the memory size control bits in the interrogation register and the ability of the 8EC252 bond-out device to execute out of the specified address space. |
| 0015H | Program to Data Memory | Verifies the operation of the 8EC252 bond-out device's data path. |
| 0016H | Bond-out Device Signature Register | Verifies that the data contained in the 8EC252 bond-out device's signature register reflects the correct bond-out type and revision levels for these diagnostics. |
| 0017H | Control Register | Verifies that setting or clearing the control bits perform their appropriate function. |
| 0018H | Program Memory (MOVC) | Verifies that the 8EC252 bond-out device can fetch code from both internal and external code memory. |
| 0019H | Instruction Set | Verifies the correct execution of all mnemonics in at least one addressing mode. |
| 001AH | Internal Memory RAM | Verifies the accessibility, address uniqueness, and data integrity of the 256 bytes (0-0FFH) of the internal RAM memory. |
| 001BH | Local 8051 Type Interrupts | Verifies that the internal timers operate correctly and that the internal and external interrupts respond correctly to the proper input stimulus. |
| 001CH | 80C252 Port 0-1/ Port 2-3 | Verifies that each port pin has continuity and can perform a read and write operation. |
| 001DH | 80C252 PCA/TMR2 Interrupts | Verifies that timer 2 and program counter array (PCA) interrupts operate correctly during internal and external interrupts. |
| 001EH | 8EC252 Host Control Signals | Verifies that the host/slave interface handshake mechanism is functional. |
| 001FH | 8EC252 RST, $\overline{EA}$ Control | Verifies that the microcontroller executes its correct function when these pins are activated or deactivated. |
| 0020H | Host-Probe Utilities (Usually Ignored) | Host-probe debug utilities are used to read and write various 8EC252 bond-out chip memories and registers. |

# B SPECIAL FUNCTION REGISTERS

Table B-1 lists the special function registers of the ICE-5100/252 user probe.

**NOTE**

The 80C252 contains a superset of the 8051 and 8052 registers. Some of the registers listed may not be available on the actual component emulated.

**Table B-1 Special Function Register Keywords**

| Register Keyword | Address | Function | Notes |
|---|---|---|---|
| $ | | Program counter | |
| ACC | 0E0H | Accumulator | 1 |
| B | 0F0H | Multiplication register | 1 |
| CCAP0H | 0FAH | PCA compare/capture 0 high | 2 |
| CCAP1H | 0FBH | PCA compare/capture 1 high | 2 |
| CCAP2H | 0FCH | PCA compare/capture 2 high | 2 |
| CCAP3H | 0FDH | PCA compare/capture 3 high | 2 |
| CCAP4H | 0FEH | PCA compare/capture 4 high | 2 |
| CCAP0L | 0EAH | PCA compare/capture 0 low | 2 |
| CCAP1L | 0EBH | PCA compare/capture 1 low | 2 |
| CCAP2L | 0ECH | PCA compare/capture 2 low | 2 |
| CCAP3L | 0EDH | PCA compare/capture 3 low | 2 |
| CCAP4L | 0EEH | PCA compare/capture 4 low | 2 |
| CCAPM0 | 0DAH | PCA compare/capture mode 0 | 2 |
| CCAPM1 | 0DBH | PCA compare/capture mode 1 | 2 |
| CCAPM2 | 0DCH | PCA compare/capture mode 2 | 2 |
| CCAPM3 | 0DDH | PCA compare/capture mode 3 | 2 |
| CCAPM4 | 0DEH | PCA compare/capture mode 4 | 2 |
| CCON | 0D8H | PCA counter control | 1, 2 |
| CH | 0F9H | PCA counter high | 2 |
| CL | 0E9H | PCA counter low | 2 |
| CMOD | 0D9H | PCA counter mode | 2 |
| DPH | 083H | Data pointer high | |
| DPL | 082H | Data pointer low | |
| IE | 0A8H | Interrupt enable | 1 |

**NOTES:**
1. These registers are both byte and bit addressable.
2. These registers are only on the 80C252.

**Table B-1 Special Function Register Keywords continued**

| Register Keyword | Address | Function | Notes |
|---|---|---|---|
| IP | 0B8H | Interrupt priority | 1 |
| P0 | 080H | Port 0 | 1 |
| P1 | 090H | Port 1 | 1 |
| P2 | 0A0H | Port 2 | 1 |
| P3 | 0B0H | Port 3 | 1 |
| PCON | 087H | Power control | |
| PSW | 0D0H | Program status word | 1 |
| RCAP2H | 0CBH | Reload/capture 2 high | 3 |
| RCAP2L | 0CAH | Reload/capture 2 low | 3 |
| SADDR | 0A9H | Serial address | 2 |
| SADEN | 0B9H | Serial address enable | 2 |
| SBUF | 099H | Serial data buffer | |
| SCON | 098H | Serial control | 1 |
| SP | 081H | Stack pointer | |
| TCON | 088H | Timer/counter control | 1 |
| T2CON | 0C8H | Timer/counter 2 control | 1, 3 |
| TL0 | 08AH | Timer/counter low 0 | |
| TL1 | 08BH | Timer/counter low 1 | |
| TH0 | 08CH | Timer/counter high 0 | |
| TH1 | 08DH | Timer/counter high 1 | |
| TL2 | 0CCH | Timer/counter low 2 | 3 |
| TH2 | 0CDH | Timer/counter high 2 | 3 |
| TMOD | 089H | Timer/counter mode | |
| T2MOD | 0C9H | Timer/counter 2 mode | 3 |

**NOTES:**
1. These registers are both byte and bit addressable.
2. These registers are only on the 80C252.
3. These registers are only on the 8052 and 80C252 microcontrollers.

# C SPECIAL FUNCTION REGISTER BITS

Table C-1 lists the special function register bits of the ICE-5100/252 user probe.

**NOTE**

The ICE-5100/252 user probe contains a superset of the 8051/52 register set. Not all of the registers/bits may be available in the component being emulated.

**Table C-1 Special Function Register Bit Keywords**

| Register Bit Keyword | Address | Function | Notes |
|---|---|---|---|
| Interrupt Enable Register | | | |
| EA | 0AFH | Enable all interrupts | |
| EC | 0AEH | PCA interrupt enable | 1, 2 |
| ET2 | 0ADH | Enable timer/counter 2 interrupt | 1 |
| ES | 0ACH | Enable serial port interrupt | |
| EX0 | 0A8H | Enable external interrupt 0 | |
| EX1 | 0AAH | Enable external interrupt 1 | |
| ET0 | 0A9H | Enable timer/counter 0 interrupt | |
| ET1 | 0ABH | Enable timer/counter 1 interrupt | |
| Interrupt Priority Register | | | |
| PPC | 0BEH | PCA interrupt priority level | 1, 2 |
| PT0 | 0B9H | Priority of timer/counter 0 | |
| PT1 | 0BBH | Priority of timer/counter 1 interrupt | |
| PT2 | 0BDH | Priority of timer/counter 2 interrupt | 1 |
| PS | 0BCH | Priority of serial port interrupt | |
| PXO | 0B8H | Priority of external interrupt 0 | |
| PX1 | 0BAH | Priority of external interrupt 1 | |
| Port 3 Register | | | |
| RXD | 0B0H | Serial port receive pin | |
| TXD | 0B1H | Serial port transmit pin | |
| INT0 | 0B2H | Interrupt 0 input pin | |
| INT1 | 0B3H | Interrupt 1 input pin | |

**NOTES:**
1. Not available in 8051 components
2. Not available in 8052 components

**Table C-1 Special Function Register Bit Keywords continued**

| Register Bit Keyword | Address | Function | Notes |
|---|---|---|---|
| T0 | 0B4H | Timer/counter 0 external flag | |
| T1 | 0B5H | Timer/counter 1 external flag | |
| WR | 0B6H | Write data for external memory | |
| RD | 0B7H | Read data for external memory | |
| Port 1 Register | | | 1, 2 |
| T2 | 090H | External clock input to timer 2 | |
| T2EX | 091H | External control input to timer 2 | |
| ECI | 092H | External clock input to PCA register | |
| CEX0 | 093H | External control I/O for register/comparator module 0 | |
| CEX1 | 094H | External control I/O for register/comparator module 1 | |
| CEX2 | 095H | External control I/O for register/comparator module 2 | |
| CEX3 | 096H | External control I/O for register/comparator module 3 | |
| CEX4 | 097H | External control I/O for register/comparator module 4 | |
| PSW Register | | | |
| P | 0D0H | Parity flag | |
| OV | 0D2H | Overflow flag | |
| RS0 | 0D3H | Register bank select 0 | |
| RS1 | 0D4H | Register bank select 1 | |
| F0 | 0D5H | Flag 0 | |
| AC | 0D6H | Auxiliary carry flag | |
| CY | 0D7H | Carry flag | |
| SCON Register | | | |
| RI | 098H | Receive interrupt flag | |
| TI | 099H | Transmit interrupt flag | |
| RB8 | 09AH | Receive bit 8 | |
| TB8 | 09BH | Transmit bit 8 | |
| REN | 09CH | Receive enable | |
| SM2 | 09DH | Serial mode control bit 2 | |
| SM1 | 09EH | Serial mode control bit 1 | |
| SM0 or FE | 09FH | Serial mode control bit 0 | |
| T2CON Register | | | 1 |
| CPRL2 | 0C8H | Capture/reload timer/counter 2 | |
| CT2 | 0C9H | Counter/timer 2 select | |
| TR2 | 0CAH | Timer/counter 2 run | |
| EXEN2 | 0CBH | External enable of timer/counter 2 | |
| TCLK | 0CCH | Transmit clock | |
| RCLK | 0CDH | Receive clock | |
| EXF2 | 0CEH | External flag timer/counter 2 | |
| TF2 | 0CFH | Timer/counter 2 overflow flag | |

**NOTES:**
1. Not available in 8051 components
2. Not available in 8052 components

**Table C-1 Special Function Register Bit Keywords continued**

| Register Bit Keyword | Address | Function | Notes |
|---|---|---|---|
| TCON Register | | | |
| IT0 | 088H | Interrupt 0 type control bit | |
| IE0 | 089H | Interrupt 0 edge flag | |
| IT1 | 08AH | Interrupt 1 type control bit | |
| IE1 | 08BH | Interrupt 1 edge flag | |
| TR0 | 08CH | Timer/counter 0 run control flag | |
| TF0 | 08DH | Timer/counter 0 overflow flag | |
| TR1 | 08EH | Timer/counter 1 run control flag | |
| TF1 | 08FH | Timer/counter 1 overflow flag | |
| CCON Register | | | 1, 2 |
| CF | 0DFH | Overflow flag for CCON register | |
| CR | 0DEH | Run control bit for CCON register | |
| | | Bit 5 not used | |
| CCF4 | 0DCH | Compare/capture status flag for CCON 4 | |
| CCF3 | 0DBH | Compare/capture status flag for CCON 3 | |
| CCF2 | 0DAH | Compare/capture status flag for CCON 2 | |
| CCF1 | 0D9H | Compare/capture status flag for CCON 1 | |
| CCF0 | 0D8H | Compare/capture status flag for CCON 0 | |

**NOTES:**
1. Not available in 8051 components
2. Not available in 8052 components

# D ICE™-5100/252 EMULATOR SUPPORT OF CHMOS AND HMOS COMPONENTS

This appendix describes differences between CHMOS and HMOS components and how the ICE™-5100/252 emulator addresses these differences.

## D.1 CHMOS AND HMOS Differences

The ICE-5100/252 user probe is based on a CHMOS component and will emulate both CHMOS and HMOS versions of the 8051 microcontroller family. This capability is possible due to the I/O structure similarities between CHMOS and HMOS components. However, the clock oscillators are not similar and deserve special attention.

As noted in the *Microcontroller Handbook*, order number 210918, operation with a crystal or other resonant device of both components is the same. The area of concern is when emulating an HMOS component using an external clock. As shown in Figure D-1, CHMOS components are driven by an external clock through XTAL1 with XTAL2 open, while HMOS components are externally driven through XTAL2 with XTAL1 connected to $V_{ss}$.

To accommodate the differences in clocking between the two types of components, jumpers were placed on the clock lines of the ICE-5100/252 processor module. The jumpers enable you to emulate both CHMOS and HMOS clock driven target systems. Table D-1 shows the possible jumper configurations for both CHMOS and HMOS components.

**NOTE**

The jumpers must be configured for CHMOS components when using the emulator in the stand-alone mode. Refer to Section 1.5 in this manual for instructions on changing the jumpers.

The following sections discuss design considerations between the two types of components and possible work-arounds.

### D.1.2 Reset

As shown in Table D-2, there are differences between CHMOS and HMOS components RST (pin 9) specifications. The differences are such that a reset is longer when the ICE-5100/252 user probe is plugged into an HMOS target socket using an RC reset circuit unless a resistor is added from RST to ground in parallel with the existing one. If RST is supplied by a TTL device that does not reach a logic high of 3.5V or more, a pull-up resistor should be added as is usually done when interfacing TTL to CMOS.

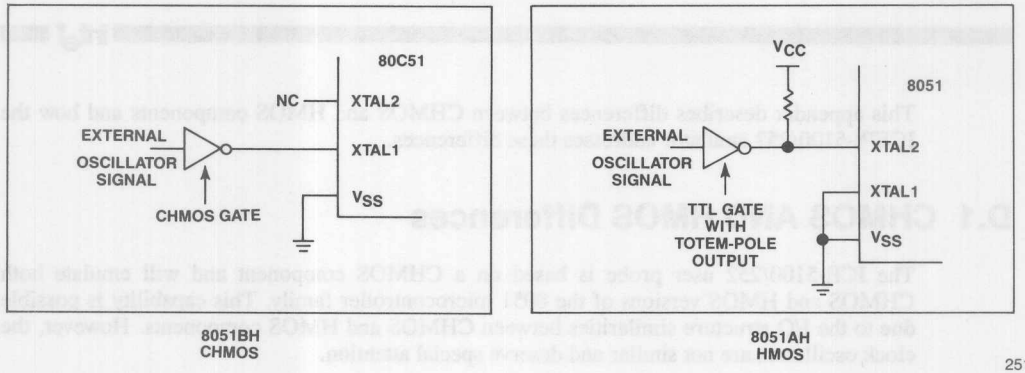



**Figure D-1 Driving CHMOS and HMOS MCS-51 Parts with an External Clock Source**

**Table D-1 Jumper Positions for CHMOS and HMOS Clock Lines**

| MCS™-51 Component | Jumpers Installed | Jumpers Removed |
|---|---|---|
| 80C51 | E5-E6 | E1-E2 |
| 80C252 CHMOS or CPA installed (stand-alone | E7-E8 | E3-E4 |
| 8051 mode) | | |
| 8051 HMOS, using a crystal or with CPA installed | E5-E6 | E1-E2 |
| 8052 | E7-E8 | E3-E4 |
| 8051 HMOS, using an external clock | E1-E2 | E5-E6 |
| 8052 | E3-E4 | E7-E8 |

**Table D-2 CHMOS vs HMOS Pin 9 Specifications**

| Function | 80C51 CHMOS | 8051AH HMOS |
|---|---|---|
| Trigger threshold | 70% $V_{CC}$ (3.5V @$V_{CC}$ = 5) | 2.5V |
| Input impedance | 50k-150K ohms | 4k-10K ohms |

### D.1.3 Ports

The logical 0 input current ($I_{il}$) of ports 1, 2, and 3 is specified as $-50\mu A$ for the 80C51 and the ICE-5100/252 user probe while $I_{il}$ for an 8051AH is $-800\mu A$.

If your target system was designed for the 80C31 or the 80C51, then the ICE-5100/252 user probe will work without any modifications. In some cases, you may have to make circuit modifications such as adding pull-up resistors to port pins for full 8051 and 8051AH functionality.

For example, if your target system uses the $-800\mu A$ $I_{il}$ of the 8031AH ports 1-3 for pull-ups, there may be problems as the ICE-5100/252 user probe's $I_{il}$ is only $-50\mu A$. A typical design where this could pose problems is an SPST keyboard connected directly to the ports via a cable. The cable capacitance would be charged at the key release by the user probe's $-50\mu A$ instead of the $-800\mu A$ provided by the 8031AH. This could slow things down by a factor of 16. Note that adding external pull-up resistors to provide more current has the side effect of using up part of the 1.6mA $I_{ol}$ of the ICE-5100/252 user probe.

## D.2 Summary

Table D-3 lists the areas of concern for CHMOS and HMOS compatibility. In most cases, adding pull-up or pull-down resistors will provide the needed compatibility.

Table D-4 summarizes the differences between CHMOS and HMOS components. Refer to the MCS-51 Architecture section in the *Microcontroller Handbook*, order number 210918, for more information on the differences between CHMOS and HMOS microcontroller components.

**Table D-3 CHMOS and HMOS Incompatibilities**

| Function | TTL Compatibility | | Pin Compatibility | | AC Specifications | | Specifications | |
|---|---|---|---|---|---|---|---|---|
| | CHMOS | HMOS | CHMOS | HMOS | CHMOS | HMOS | CHMOS | HMOS |
| Reset | no | no | yes | yes | same | | different | |
| Clock | no | no | no | no | 16 MHz | 12 MHz | different | |
| Ports | same | | yes | yes | same | | different | |

**Table D-4 CHMOS and HMOS Design Differences**

| Chip Function | HMOS Component 8051 | CHMOS Component 80C51 |
|---|---|---|
| RST trigger threshold | 2.5V | 70% $V_{cc}$ (3.5V @ $V_{cc}$ = 5V) |
| RST input impedance | 4K - 10K ohms | 50K - 150K ohms |
| Port $I_{il}$ | $-800\mu A$ | $-50\mu A$ |
| Clock threshold | 2.5V | 70% $V_{cc}$ (3.5V @ $V_{cc}$ = 5V) |

The **boldface** indicates the primary reference.